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HIGH SPEED MULTI-LEVEL DISCRETE WAVELET TRANSFORM USING CANONIC SIGNED DIGIT TECHNIQUE

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ABSTRACT

A few designs have been proposed for productive VLSI usage of 2-D DWT for continuous applications. It is discovered that multipliers expend more chip zone and builds unpredictability of the DWT engineering. Multiplier-less (M-less) equipment usage approach gives an answer for lessen chip zone, bring down equipment unpredictability and higher throughput of calculation of the DWT architecture.

The proposed design outline is (i) priority must be given for memory complexity optimization over the arithmetic complexity optimization or reduction of cycle period and (ii) memory utilization efficiency to be considered ahead of memory reduction due to design complexity of memory optimization method. Based on the proposed design outline four separate design approaches and concurrent architectures are presented in this thesis for area-delay and power efficient realization of multilevel 2-D DWT.

In this theory a M-less VLSI engineering is proposed utilizing new circulated math calculation named CSD. We show that CSD is an exceptionally effective design with adders as the primary part and free of ROM, duplication, and subtraction. The proposed engineering utilizing CSD gives less deferral and least number of cut looked at the current design.

The simulation was performed using XILINX 14.1i and ModelSim simulator

KEYWORDS: 2-D Discrete Wavelet Transform (DWT), CSD, Low Filter Bank, High Filter Bank, Xilinx Simulation.

1. INTRODUCTION

The DWT is computationally escalated and the majority of its application request ongoing preparing. One method for accomplishing rapid execution is to utilize quick computational calculation in broadly useful PCs. Another path is to abuse the parallelism natural in the calculation for simultaneous handling by an arrangement of parallel processor. Yet, it isn't practical to utilize a broadly useful PC for a particular application. Likewise, broadly useful PC utilized for their execution required more space, expansive power and more calculation time. With the improvement of extensive scale incorporation (VLSI) innovation it encourages to computerized flag handling (DSP) framework architect to outline an elite, minimal effort and low power framework in a solitary chip. The normal for VLSI framework are that they offer more noteworthy potential for substantial measure of simultaneousness and offer a huge measure of processing power inside a little territory [1, 2]. The calculation is exceptionally shoddy as the equipment isn't a deterrent for VLSI framework. In any case, the non-restricted worldwide correspondence isn't just costly yet requests high power dispersal. Along these lines, a high level of parallelism and a closest neighbor correspondence are essential for acknowledgment of superior VLSI framework [3]. Keeping this in see, elite application particular VLSI frameworks are quickly developing as of late. The exceptional reason VLSI frameworks augment preparing simultaneousness by parallel/pipeline handling and gives savvy contrasting option to constant application. In this manner, 2-D DWT is presently executed in a VLSI framework to meet the transient necessity of ongoing application. Keeping this reality in see, a few plan plans have been recommended over the most recent two decades for effective execution of 2-D DWT in a VLSI framework. Analysts have received diverse calculation plan, mapping plan, and compositional outline strategies to lessen the computational time, number-crunching intricacy or memory many-sided quality

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of 2-D DWT structures. In any case, the territory defers execution of the current structures changes barely. This is mainly due to the memory complexity, which forms a major hardware component of folded 2-D DWT structure [4].

Presently multi day, the greater part of the data in Computer preparing is dealt with on the web. This online data is either graphical or pictorial in nature, and the capacity and correspondence necessities are huge [5]. Subsequently technique for packing the information preceding capacity and transmission are of noteworthy down to earth and business intrigue. Picture pressure implies lessening the excess measure of information required to speak to an advanced picture. The Digital picture pressure in numerical shape can be characterized as change of a 2-D pixel cluster by picture, into a measurably uncorrelated informational collection. The change is connected on picture preceding capacity and transmission of Digital Image Data. The compacted picture is remade into unique picture by the procedure of Decompression [6]. Decompressed picture can be a unique picture or estimation of it [7]. Picture pressure is the innovation for dealing with the expanded spatial goals of the present imaging sensors and developing communicate TV guidelines. Picture pressure assumes a critical part in numerous essential and differing applications including tele video conferencing, remote detecting, report and therapeutic imaging, copy transmission and the control of remotely steered vehicles in military, space, and dangerous waste administration applications [8]. The application list is regularly developing the effective control stockpiling and transmission of various sorts of computerized picture, for example, parallel pictures, dim scale pictures, and shading pictures and so on.

2. MULTI RESOLUTION ANALYSIS(MRA)

Despite the fact that the time and recurrence goals issue are consequence of physical marvel (the Heisenberg Uncertainty Principle) and exists paying little heed to the change utilized, it is conceivable to break down any flag by utilizing. MRA, as the name infers, breaks down the flag at various frequencies with various goals. Each unearthly segment isn't settled similarly just like the case in the STFT [9]. MRA is intended to give great time goals and poor recurrence goals at high frequencies and great recurrence goals and poor time goals at low recurrence. This approach bodes well particularly when motion close by has high recurrence segments for brief spans and low recurrence segments for long terms for instance flag like non-stationary flag as appeared in figure 1 and the time recurrence goals as appeared in figure 2. Luckily, the signs that are experienced in commonsense applications, specifically on account of sound, are regularly of this compose [10, 11].

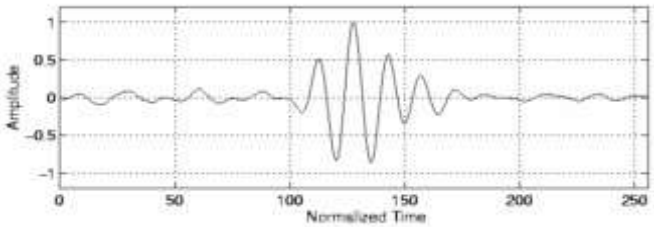

Figure 1: Non-stationary Signals

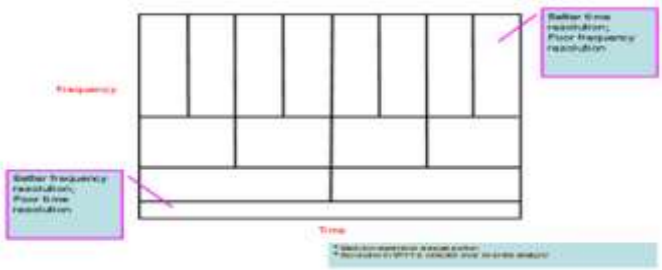

Figure 2: Resolution of Time & Frequency

Wavelet changes (WT) defeat the previously mentioned goals issue [12]. Each case in Figure 3 has a steady territory and consequently speaks to measure up to segments of the time - recurrence plane, yet extraordinary

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extents are apportioned to time and recurrence. The short high-recurrence premise capacities and the long low-recurrence ones empower point by point time and recurrence investigation to be performed in the meantime [13]. To put it plainly, the wavelet change is very much confined in recurrence and time. The information can likewise be prepared on various scales or goals not at all like the settled goals of the STFT.

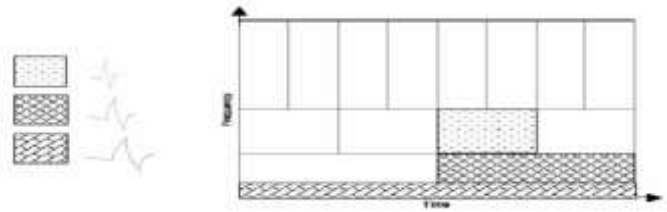

Figure 3: Time-frequency plane of a Wavelet Transform

3. PROPOSED ARCHITECTURE

Inner product computation can be expressed by CSD. The DWT formulation using convolution scheme given in can be expressed by inner product, where the 1-D DWT formulation given in (1) – (2) cannot be expressed by inner product. Although, convolution DWT demands more arithmetic resources than DWT, convolution DWT is considered to take the advantages of CSD-based design. CSD formulation of convolution-based DWT using 5/3 biorthogonal filter is presented here.

According to (1) and (2), the 5/3 wavelet filter computation in convolution form is expressed as

$$Y_L = \sum_{i=0}^{4} h(i) X_n(i) \quad (1)$$

$$Y_H = \sum_{i=0}^{2} g(i) X_n(i) \quad (2)$$

The low-pass (LP) coefficients {h(i)} and high-pass (HP) coefficients {g(i)} of the 5/3 wavelet filter coefficient. Y_H is the HPF output and Y_L is the LPF output

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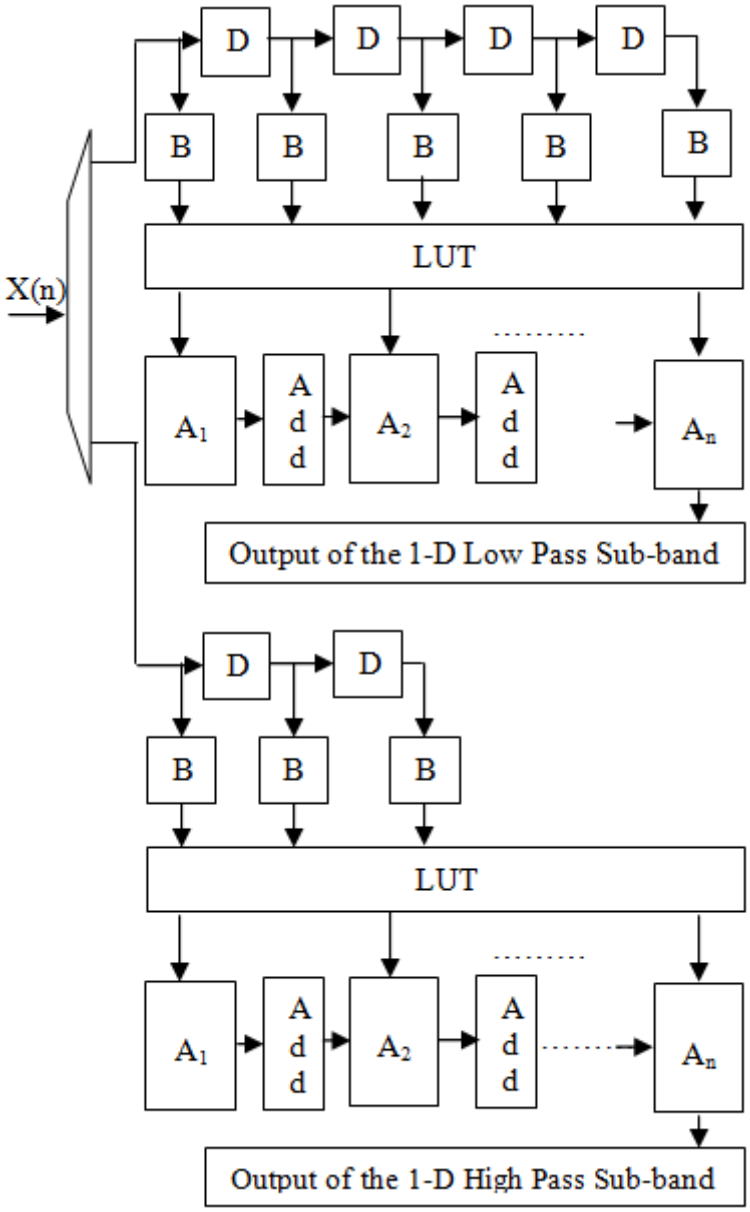

Figure 4: Block Diagram of 5/3 1-D DWT using CSD Technique

Where
B: Buffer
D: Delay flip flop
A_1: First output of the LUT
A_2: Second output of the LUT and add '0'
A_n: N output of the LUT and add (N-1) zero bit

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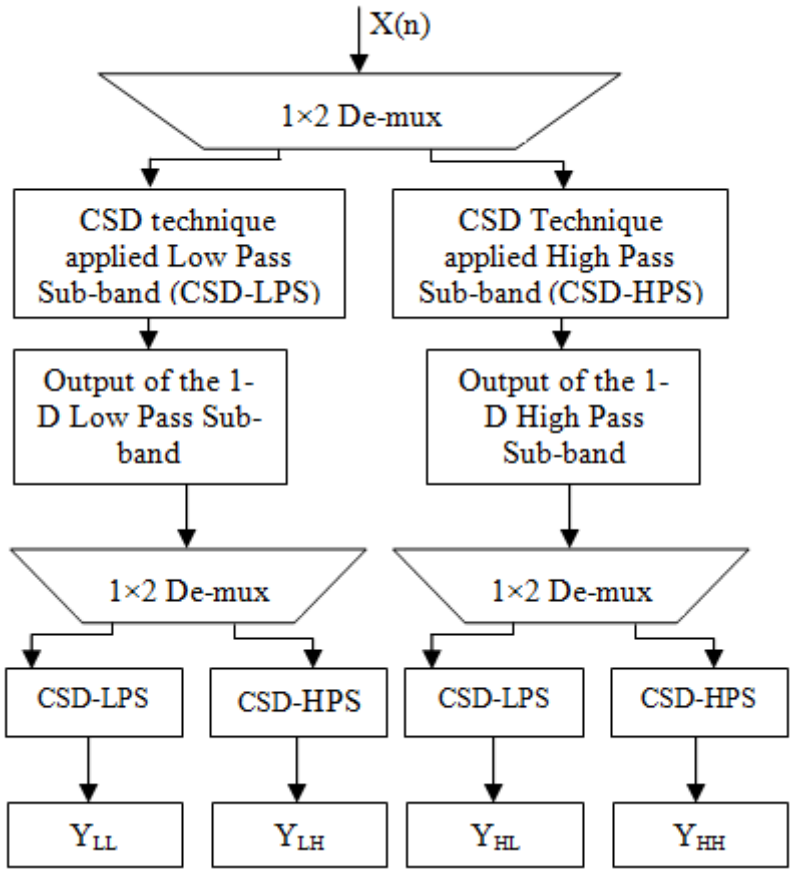

Figure 5: Block Diagram of 5/3 2-D DWT using CSD Technique

Where
Y_{LL} is the low-low output
Y_{LH} is the low-high output
Y_{HL} is the high-low output
Y_{HH} is the high-high output

4. RESULT AND SIMULATION

A. Synthesis Utilization

Device utilization summary for 1-D and 2-D DWT using CSD technique are shown in table I and table II respectively. From the table I, that the processing unit for 5/3 1-D DWT using CSD technique uses 99 number of slice registers, 1164 number of 4-input look up table (LUTs), 68 LUT flip flop, 74 number of input output bounds (IOBs), 1.552 nsec minimum period, 644.330 MHz maximum frequency and 10.162 nsec maximum combination path delay. The processing unit for 5/3 2-D DWT using CSD technique uses 236 number of slice registers, 1453 number of 4-input LUTs, 148 LUT flip flop, 88 number of input output bounds (IOBs), 3.591 nsec minimum period, 278.489 MHz maximum frequency and 12.368 nsec maximum combination path delay.

B. Comparision Result

As shown in table I the maximum frequency and number of slice result are obtained for the proposed 5/3 2-D DWT using CSD algorithm and previous algorithm. From the analysis of the results, it is found that the proposed 5/3 2-D DWT using CSD algorithm gives a superior performance as compared with previous algorithm.

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The proposed algorithm gives a maximum frequency 190.54 MHz for Virtex-5 device family as compared with 365 MHz for previous algorithm. Similarly, proposed algorithm gives a lower number of slices 236 for Virtex-5 device family and 1235 for Virtex-4 device family as compared with 1261 for Virtex-5 device family and 2278 for Virtex-4 device family for previous algorithm.

Table I: Device utilization summary for 1-D DWT using CSD Technique

Parameter	Used
Number of Slice	527
Number of Slice Flip Flop	79
Number of LUTs	946
MP	1.819 nsec
MF	549.753 MHz
MCPD	13.501 nsec

Table II: Device utilization summary for 2-D DWT using CSD Technique

Parameter	Used
Number of Slice	2750
Number of Slice Flip Flop	416
Number of LUTs	5011
MP	7.271 nsec
MF	137.535 MHz
MCPD	25.099 nsec

The proposed algorithm gives a slice register 236 for Virtex-5 device family as compared with 645 for previous algorithm. Similarly, proposed algorithm gives lower slices LUTs 1453 for Virtex-5 device family and as compared with 5485 for previous algorithm is shown in table II.

MP: Minimum Period
MP: Maximum Frequency
MCPD: Maximum Combinational Path Delay

Table III: Previous and Implemented Algorithm Compared Result

Parameter	**1-D DWT**		**2-D DWT**	
	Previous Design	Proposed Design	Previous Design	Proposed Design
Number of Slice	599	527	3264	2750
Number of Slice Flip Flop	97	79	496	416
Number of LUTS	1049	946	5579	5011
MCPD	16.146 ns	13.501 ns	31.998 ns	25.099 ns

5. CONCLUSION

In this paper, CSD-based architecture for computation of 1-D and 2-D DWT is presented. The proposed CSD-based 1-D DWT structure involves significantly less logic resources than the similar existing multiplier-less designs and, it has less bit-cycle period than others.

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The proposed CSD-based 2-D DWT architectures (architecture-1 and architecture- 2) involve the same logic components but they differ with on-chip memory size and frame buffer size. The architecture-1 is based on line-scanning and the architecture-2 is based on parallel data access scheme.

REFERENCES

[1] Samit Kumar Dubey, Arvind Kumar Kourav and Shilpi Sharma, "High Speed 2-D Discrete Wavelet Transform using Distributed Arithmetic and Kogge Stone Adder Technique", International Conference on Communication and Signal Processing, April 6-8, 2017, India
[2] Rakesh Biswas, Siddarth Reddy Malreddy and Swapna Banerjee, "A High Precision-Low Area Unified Architecture for Lossy and Lossless 3D Multi-Level Discrete Wavelet Transform", Transactions on Circuits and Systems for Video Technology, Vol. 45, No. 5, May 2017.
[3] Satish S Bhairannawar, Rajath Kumar, "FPGA Implementation of Face Recognition System using Efficient 5/3 2D-Lifting Scheme", 2016 International Conference on VLSI Systems, Architectures, Technology and Applications (VLSI-SATA).
[4] Maurizio Martina, Guido Masera, Massimo Ruo Roch, and Gianluca Piccinini, "Result-Biased Distributed-Arithmetic-Based Filter Architectures for Approximately Computing the DWT", IEEE Transactions on Circuits and Systems—I: Regular Papers, Vol .62, No.8, and August 2015.
[5] S.G. Mallat, "A Theory for Multiresolution Signal Decomposition: The Wavelet Representation", IEEE Trans. on Pattern Analysis on Machine Intelligence, 110. July1989, pp. 674-693.
[6] M. Alam, C. A. Rahman, and G. Jullian, "Efficient distributed arithmetic based DWT architectures for multimedia applications," in Proc. IEEE Workshop on SoC for real-time applications, pp. 333 336, 2003.
[7] Senthil singh C and Manikandan. M, "Design and Implementation of an FPGA-Based Real-Time Very Low Resolution Face Recognition System", International Journal of Advanced Information Science and Technology, Vol. 7, No. 7, pp. 59-65, November 2012.
[8] Archana Chidanandan and Magdy Bayoumi, "Area-Efficient MDA Architecture for the 1-D DCT/IDCT," ICASSP 2006.
[9] M. Martina, and G. Masera, "Low-complexity, efficient 9/7 wavelet filters VLSI implementation," IEEE Trans. on Circuits and Syst. II, Express Brief vol. 53, no. 11, pp. 1289-1293, Nov. 2006.

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